Fig. 1

1: controller

11: lower device controlling system

11a: command transmission data input processing

11b: command execution result display processing

11c: communication processing

12: operating system

3: lower device

31: memory IC function estimation system

31a: command analyzing processing

31b: memory IC function test processing

31c: memory IC function test execution controlling processing

31d: timer interruption processing

31e: random number generation processing

31f: transmission data edit processing

31g: communication processing

32: real time operating system

4: input device

5: display device

Fig. 2

31b: memory IC function test processing

31b1: memory IC function test No 1 processing

31b2: memory IC function test No 2 processing

31b(n-1): memory IC function test No (n-1) processing

31bn: memory IC function test No (n) processing

Fig. 3

Operation procedure in the controller 1

STEP 1: Enter the test NO for the estimation of the memory IC

Enter Key input?

STEP 2: Transmit the transmission data corresponding to the test NO for the estimation of the memory IC, to the lower device 3

STEP 3: Display the memory IC estimation execution result received from the lower device 3

End

Fig. 3

Operation procedure in the lower device 3

There exists the received data?

STEP 4: Analyze the received data according to the command analyzing processing 31a

Test of memory ICs is executed?

STEP 5: Execute the corresponding memory IC function test 31b

Execute the estimation tests of the memory ICs

STEP 6: Transmit the execution result to the controller 1 after the end of the test

End

Fig. 5

Estimation test of memory ICs

STEP 7: Take out the numeric value t1 according to the random number generation processing 31e

STEP 8: Activate the timer interruption processing 31d with the cycle of t1 millisecond

STEP 9: Activate the memory IC function test processing 31b1 for the estimation of the first memory IC

End of the memory IC function test?

End

Fig. 6

Timer interruption processing of the cycle t1

All the memory IC tests are finished?

STEP 10: Interrupt the memory IC function test processing 31b1 executing the estimation test of the first memory IC, according to the memory IC function test execution controlling processing 31c and activate the estimation test of the second memory IC according to the memory IC function test processing 31b2

Take out the numeric value t2 according to the random number generation processing 31e

STEP 11: Activate the timer interruption processing 31d with the cycle of t2 millisecond

End

Fig. 7

Timer interruption processing of the cycle t(n-1)

All the memory IC tests are finished?

STEP 12: Interrupt the memory IC function test processing 31b(n-1) executing the estimation test of the (n-1)-th memory IC, according to the memory IC function test execution controlling processing 31c and activate the estimation test of the n-th memory IC according to the memory IC function test processing 31bn

Take out the numeric value tn according to the random number generation processing 31e

STEP 13: Activate the timer interruption processing 31d with the cycle of tn millisecond

End

Fig. 8

Timer interruption processing of the cycle tn

All the memory IC tests are finished?

STEP 14: Interrupt the memory IC function test processing 31bn executing the estimation test of the n-th memory IC, according to the memory IC function test execution controlling processing 31c and activate the estimation test of the first memory IC according to the memory IC function test processing

31b1

Take out the numeric value t(n+1) according to the random number generation processing 31e

STEP 15: Activate the timer interruption processing 31d with the cycle of t(n+1) millisecond

End

Fig. 9

Execute the SRAM test 1(W/R/C test) under the following conditions.

pa: access start address

pb: access end address

pc: access type

pe: test data (1: increment data/2: fixed data)

pg: execution time, once

ph: there is/isn't display during execution (1: no display/2: display)

pi: operation in the event of error generation (1: stop/2: continue)

Upon receipt of the "END" command during the execution of the test, the current executing test is cancelled and finished.

Fig. 10

Number of execution times

Number of error generation times